UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,051	04/13/2004	Kramadhati V. Ravi	42P8813XD	6109

8791 7590 10/18/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,051	RAVI, KRAMADHATI V.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bendik et al. (US 5,591,678) in view of Okojie (US 6,248,646).

Regarding claim 1, Bendik et al. discloses in figure 2 an apparatus comprising a plurality of circuit substrates 46a, 46, 46b and the plurality of circuit substrates are in a non-planar orientation relative to one another (elements 46a, 46, 46b are clearly in non-planar orientation) stacked one on the other, each circuit substrate 46 comprising a single crystal semiconductor layer having smallest dimension reduced (col. 4, lines 10-15); circuit devices 50a, 50, 50b formed in the single crystal layer of each of the plurality of circuit substrates; and a plurality of interconnects 56 (col. 7, lines 1-2) disposed between the plurality of circuit substrates.

It is noted that the phrase" a single crystal semiconductor layer having a smallest dimension reduced" is a broad limitation and herein interpreted as the single crystal semiconductor layer 46 being thinned to a certain thickness as disclosed in col. 4, lines 10-15 of Bendik et al.

Bendik et al. does not a plurality of circuit substrates on a substrate. However, Okojie discloses in figure 2 the plurality of circuit substrates 24 on a substrate 20 (col. 2, lines 63-64). It is further noted that wafers 24 of Okojie are hereby considered "circuit substrates" on which semiconductor elements will be formed. In view of such teaching, it would have been obvious at the time of the present invention to modify Bendik et al. by including the plurality of circuit substrates on a substrate in order to enable an array of circuit substrates to be concurrently produced on a larger, industry standard sized wafer (substrate) and to consequently increase production rates.

Regarding claim 4, Bendik et al. discloses in figure 3 the circuit devices form integrated circuits 70b, 74 that interact with other electrical devices off the single crystal layer on which the integrated circuits are formed (col. 7, lines 29-31).

Regarding claim 5, Okojie discloses the smallest dimension of each circuit substrate 24 comprises a thickness less than 100 microns (col. 3, lines 33-36).

Regarding claim 6, Bendik et al. discloses a dielectric material 44 (col. 4, line 5) disposed between the adjacent ones of the plurality of circuit substrates 46a, 46, 46b.

Response to Arguments

Applicant's arguments filed on 09/29/2006 have been fully considered but they are not persuasive.

With respect to claim 1, applicant argues Bendiki et al. does not disclose the circuit substrate consists of a single crystal semiconductor layer as recited in now amended claim 1. It is well known in the art that the substrate is defined as "a

supporting material on or in which the components of an integrated circuit being fabricated or attached". Element 46 as shown in figure 2 of Bendik et al. is a supporting material on which the circuit component 50 of an integrated circuit is fabricated. As such, elements 46a, 46, 46b alone can be construed as "the circuit substrates" and each of these circuit substrates consist of a single crystal semiconductor layer (col. 4, lines 10-12). It is noted that elements 44 (stop etch layers) are necessarily not part of the so-called circuit substrate in this broad interpretation. Therefore, the combination of Bendik et al. and Okojie reads on claim 1 herein. Since the rejection of claim 1 is proper, the rejection of dependent claims 4-6 still stands.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
October 16, 2006.

KENNETH PARKER
SUPERVISORY PATENT EXAMINER